Least Squares Modeling of Voltage Harmonic Distortion Due to PC Cluster Operation

Saša MUJOVIĆ[1], Slobodan DJUKANOVIĆ[1], Vladan RADULOVIĆ[1],
Vladimir KATIĆ[2], Mladen RAŠOVIĆ[1]
[1]*University of Montenegro, Faculty of Electrical Engineering, 81000 Podgorica, Montenegro*
[2]*University of Novi Sad, Faculty of Technical Science, 21000 Novi Sad, Serbia*
sasam@ac.me

***Abstract*—Regarding the possibility of harmonic generation, personal computers (PCs) are very significant within the category of non-linear low power loads. In modern distribution systems, the number of PCs simultaneously connected to distribution grid constantly increases. This PC clustering can negatively affect the quality of supply. The paper deals with mathematical modeling of the voltage total harmonic distortion (THD_U) caused by operation of PC cluster. The proposed model is based on the power quality measurements carried out in a computer centre and computer simulations. It takes into account the THD_U dependence on the PC cluster size and grid stiffness. Model parameters are derived in the least squares sense. The influences of cable cross-section and pre-existing THD_U of the phase voltage are also discussed. The accuracy of the proposed model is confirmed by additional measurements performed in a commercial building.**

***Index Terms*—Load modeling, Total harmonic distortion, Voltage measurement.**

I. INTRODUCTION

Low power electronics or microelectronics loads, based on the AC/DC power conversion, draw current with distorted or even discontinuous waveform during AC voltage cycle. Individually, these loads produce small amounts of harmonic current. However, when operating in large numbers, they have the capability of high current harmonic emission that overload neutral conductors and transformers, and cause voltage harmonic distortion, additional losses and reduction of power factor [1].

With the introduction of smart grids in power systems and further rapid advancement in electronic and information technologies, the use of such devices in customers' installations is expected to increase [2], [3]. Therefore, utility companies are very interested in ensuring that the potential harmonic effects do not jeopardize the voltage quality, where harmonic state estimation [4], [5], and load-profile analysis [6] play crucial role.

Personal computers (PCs) are, regarding harmonic emission, very important within the category of non-linear low power loads. Modern PCs use switching regulators, or switch mode power supplies, to convert the utility AC power to controlled DC power [7]. During the conversion, strong third, fifth and other odd harmonics are generated, resulting in total current harmonic distortion (THD_I) of individual PCs up to THD_I=120% [8], [9].

Application of PCs in modern distribution systems very often requires their use in large numbers. Frequently, numerous PCs are connected simultaneously to distribution grid forming a kind of cluster. Operation of a PC cluster distorts input current waveform [10]. Distorted current produces harmonic voltage drops on system impedance and results in voltage harmonic at the supply buses. Such a case is shown in Fig. 1, where a group of connected PCs produces harmonic voltage drop on equivalent system impedance (Z_e):

$$Z_e = Z_{net} + Z_L + Z_{Be}, \quad Z_{Be} = \left(\sum_{i=1}^{N} \frac{1}{Z_{Bi}} \right)^{-1}. \tag{1}$$

where Z_{net} is the network impedance, Z_L the line impedance, Z_{Bi} the impedance of the i-th branch, Z_{Be} the equivalent branch impedance and N is the number of PCs in cluster.

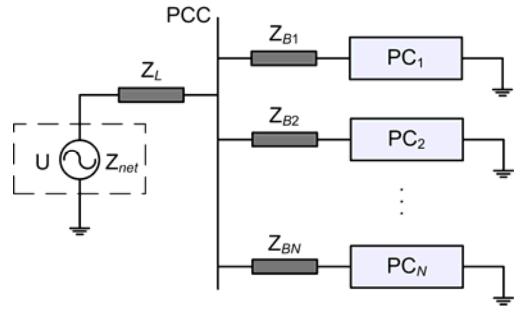

Figure 1. *N* PCs connected to the common bus.

The cluster operation results in voltage deviation from sinusoidal shape, i.e., in increasing voltage harmonic

$$U_h = Z_e I_h = (R_e + jhX_e) I_h, \tag{2}$$

where h is the harmonic order, R_e and X_e are active and reactive parts of equivalent system impedance, respectively, and I_h is the root mean square (RMS) value of the h-th harmonic current of PC cluster.

The key indices quantifying voltage distortion are total and individual harmonic distortion of voltage, THD_U and HD_U, respectively, defined as

$$THD_U = \sqrt{\frac{\sum_{h=2}^{\infty} U_h^2}{U_1^2}} 100, \quad HD_U = \frac{U_h}{U_1} 100, \tag{3}$$

where U_1 and U_h are the RMS values of the fundamental and the h-th harmonic voltage, respectively. These values are given in percentage.

Knowing the PC cluster's THD_U level is of great importance, since the comparison of the THD_U level with its limits, presented in standards [11] and [12], may provide insight into potential negative effects of PC cluster operation on voltage quality.

Measurements of power quality parameters, carried out at

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selected buses in the distribution network, represent the most precise method for the THD_U determination [13]. However, this approach requires special instrumentation, manpower, dedicated software and financial resources. Also, it reflects the state of the network, present loads and level of voltage and current harmonic that correspond to the measurement period. Any change in load characteristics, size of cluster or any other parameter afterwards, requires repeated measurements and prolonged monitoring.

In order to avoid these shortcomings, this paper deals with mathematical modeling of the THD_U. Namely, a mathematical model for the THD_U determination as a function of the number of connected PCs (N_{PC}) and other related influential parameters is derived. The proposed model is grounded on measurements, conducted at the Computer Centre of the Faculty of Technical Sciences (CCFTS) of the University of Novi Sad, and simulation results, obtained by developed Matlab simulation models of single PC and PC cluster. Its accuracy is confirmed with additional measurements performed in a commercial building (bank).

The model enables the THD_U calculation for an arbitrary PC cluster size without using expensive simulation software or sophisticated measuring apparatus. It is, therefore, highly suitable for engineering practice.

II. Background

The voltage distortion is an essential topic in power quality analysis. It is result of harmonic current emission of various non-linear loads, as explained in the introduction, and operation of power electronics converters, used for integration of renewable energy sources and energy storage devices [14], [15]. Also, advanced application of power electronics in electrical energy transmission and in high voltage DC transmission brings additional harmonic distortion in networks [16].

Numerous papers investigate the voltage distortion caused by nonlinear loads [1-3], [17-22]. Generally, these papers are oriented to the presentation of individual and/or group impact of these loads on voltage supply quality. However, only few papers deal with the THD_U on common buses supplying only PCs [1], [21], [22]. Measurement results of voltage and current distortion given in [1] and [21] present “case study”, which considers the impact of 109 PCs (around 35 PCs per phase). Therefore, these results do not have general validity for various grid characteristics.

The impact of simultaneous operation of 120 PCs (around 40 per phase) on the THD_U level through a simulation model is considered in [22]. Also, the THD_U estimation when more PCs are considered, namely 240 and 800 PCs, is given. The simulations show that the THD_U increases as the PC cluster size increases. However, the proposed model is not complete since it does not take into account all influencing parameters, including the grid stiffness and some internal PC parameters.

To our best knowledge, only one paper offers mathematical models for the THD_U calculation [23]. In particular, two models, linear and exponential, are introduced in [23] as follows:

$$THD_U = 0.002 I_L + 0.5417, \tag{4}$$

$$THD_U = 0.747 \exp(0.0014 I_L). \tag{5}$$

Models (4) and (5) enable the THD_U calculation in dependence on the connected load current (I_L), given per unit in the above relations. However, the models are derived for low voltage buses supplying not only PCs, but also other small loads (lamps, small motors, heaters). In that sense, these models are not appropriate for determination of the THD_U that is exclusively caused by the operation of a PC cluster, which is the main concern of this paper.

Model that considers the impact of PC cluster on the THD_U should incorporate dependence on the PC cluster size. In addition, research on the impact of the grid stiffness (S_{SC}) on the THD_U reveal that the THD_U is strongly affected by S_{SC}, imposing the necessity to include this dependence in model as well. Namely, it is stated in [8] that, for the same N_{PC}, the THD_U decreases with increase of S_{SC}. This statement is supported by measurements carried out at the CCFTS, in 2003 and 2010. In 2003, the measurements were conducted at the point of common coupling (PCC) from which a group of 109 PCs is supplied. The maximal recorded THD_U value was THD_U =4.8%. In 2010, the PC cluster size was around 170 PCs and the maximal recorded value of THD_U was THD_U =5.3%. Analyzing these results, a wrong conclusion can be drawn that connection of additional 61 PCs on the PCC causes negligible increase of the THD_U. However, the increase of the grid stiffness on the PCC, which happened between 2003 and 2010, is the actual cause of such a low THD_U increase.

Aside from N_{PC} and S_{SC}, minor dependence of the THD_U on several other factors, such as the cable cross-section and the initial THD_U of the phase voltage at no-load state, is observed.

III. Measurements and Simulation Results

A. Measurement Results

The CCFTS was established in late eighties of the 20th century. As the number of PCs in the CCFTS started to grow, a question of their possible negative influence on the network and other consumers has emerged. Besides harmonic emission problems, additional negative effects such as fuse blowing, cable-end overheating and high neutral current were noticed. Such problems have initiated detailed research based on the measurements of the power quality parameters and development of adequate simulation model of the CCFTS. Therefore, several measuring sessions were conducted during 2003-2010. The results of the last one were the basis for development of the model.

Measurements were conducted at the PCC from which a group of 163 PCs (153 personal PCs and 10 server PCs of total active power of 28.1 kW) were supplied. The short-circuit current (I_{SC}) at the PCC was I_{SC} = 6kA and averaged full load current of the CCFTS was I_L = 35.2A. Knowing the value of the transformers’ nominal power and its relative short-circuit voltage, the grid stiffness of S_{SC} = 4000 kVA was calculated.

The recorded phase voltage waveforms at the PCC are presented in Fig. 2. A ”flat top” of the sine wave shape is a consequence of simultaneous operation of 57, 50 and 56 PCs at phases 1, 2 and 3, respectively. In addition to PCs, the harmonic emission at the PCC comes from fluorescent lamps (out of total fluorescent lamps load of 1.6 kW, a part of 864 W was turned on during the measurement period). A detailed description of the measurement procedure can be found in [9].

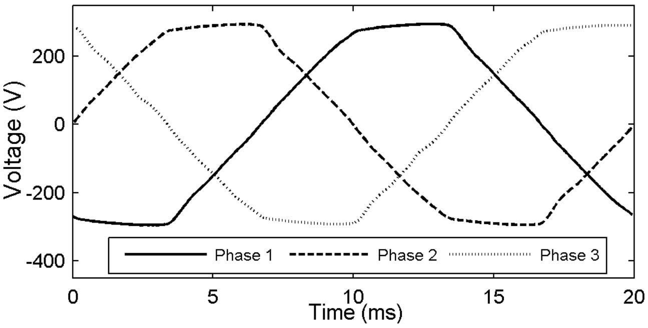

Figure 2. Voltage waveforms supplying a group of 163 PCs.

As opposed to the phase current harmonic spectra, the presence of high order harmonics in voltage spectra is not significant. Only the 5th harmonic is above the limit (3%) defined by the IEEE 519 Standard [12]. However, according to the EN 50160 Standard [11], that permits the value of odd harmonic of 6%, the level of the 5th harmonic in our case is quite satisfactory. The maximal recorded THD_U values of phase voltages were 5.18%, 5.26% and 5.30%, respectively. These values exceed the limit defined by the IEEE 519 Standard, but are considerably below the limit of the EN 50160 Standard (8%).

B. Simulation Results

A Matlab/Simulink model of the CCFTS has been developed. A full description of the simulation model and confirmation of its accuracy and adequacy is presented in [9].

The recorded values of the pre-existing (initial) THD_U at the PCC were 2.25%, 2.18% and 2.1%, per phases 1, 2, 3, respectively. The simulation model takes these values into account by setting the amplitudes and phase angles of supply voltage harmonics to the values recorded by measuring device. Hence, the supply voltage harmonics are not in phase with PC-generated harmonics at the same frequency, and the impact of attenuation and diversity is not neglected, representing real grid conditions.

IV. Proposed Model

The THD_U values, obtained by measurements and simulations performed for N_{PC} in the range of 10 to 200 PCs per phase and S_{SC}={3000, 4000, 5000, 6000, 7000} kVA, are presented in Fig. 3. Note that there is no upper limit for N_{PC}, but the selected PC cluster size is sufficient for analysis and conclusions. Also, the adopted S_{SC} range covers the most common S_{SC} values characteristic to PCCs at which the PC cluster is connected. As a matter of fact, the grid stiffness of 3000 kVA is rarely encountered, but it is included so as to make the analysis more general.

From Fig. 3, the following observations hold:

- THD_U increases as N_{PC} increases. This is due to generated current of the PC cluster. Namely, as N_{PC} increases, the PC cluster draws more current from the mains and voltage distortion increases.
- THD_U decreases as S_{SC} increases. Greater grid stiffness means greater grid capability to withstand the negative impact of generated harmonics.
- The THD_U dependence on N_{PC} is not uniform within the considered N_{PC} interval, and it can be divided into three regions. At certain number of connected PCs, the THD_U function changes its behavior and further increasing of cluster size will result in a more pronounced THD_U growth.
- As S_{SC} increases, the middle region narrows and shifts towards higher N_{PC} values. For very large S_{SC} values, it practically vanishes, and the THD_U function tends to be uniform within the whole N_{PC} interval (see the THD_U curve for S_{SC}=7000).
- Within each region, the THD_U can be well approximated by a linear function of N_{PC}.

Taking these observations into consideration, the THD_U can be modeled as

$$THD_U(N_{PC}, S_{SC}) = f(S_{SC})N_{PC} + g(S_{SC}) \,. \tag{6}$$

Our aim will be to determine functions $f(S_{SC})$ and $g(S_{SC})$ for each region, as well as the middle region boundaries $LB(S_{SC})$ and $RB(S_{SC})$. LB and RB stand for the left and right bounds of the middle region, respectively.

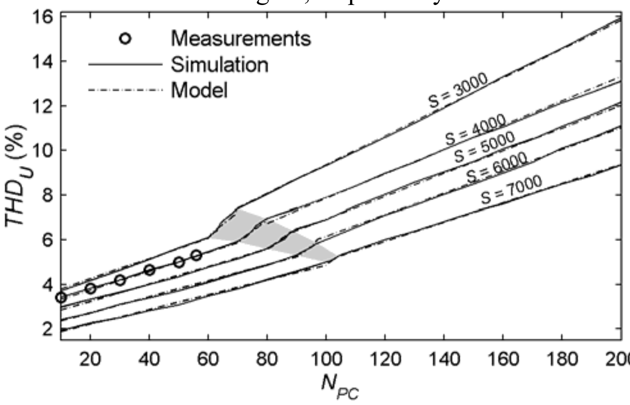

Figure 3. Simulated THD_U values (solid line) for five considered S_{SC} values. Circles denote the measurements. In the middle region (shaded), the THD_U function changes its behavior. THD_U model values, obtained by using (17), are shown by dashdot lines.

A. Estimation of Model Parameters

In this paper, functions $f(S_{SC})$ and $g(S_{SC})$ will be modeled by polynomials. The choice of polynomial model is motivated by the Weierstrass's theorem, which states that any continuous function can be approximated by a polynomial within the considered interval. In addition, polynomial model is much more appropriate for analysis compared to exponential or some other model. Analytically

$$f(S_{SC}) \approx \sum_{i=0}^{P} k_i S_{SC}^i, \qquad g(S_{SC}) \approx \sum_{j=0}^{Q} c_j S_{SC}^j, \tag{7}$$

where P and Q represent the polynomial orders, while k_i and c_j represent polynomial coefficients. The modeling problem now reduces to the estimation of parameters P, Q, k_i (i=0,1,…,P) and c_j (j=0,1,…,Q). Middle region boundaries $LB(S_{SC})$ and $RB(S_{SC})$ will also be approximated by polynomials.

1) *Estimation of $f(S_{SC})$ and $g(S_{SC})$*

For the sake of convenience, indices in N_{PC} and S_{SC} will be dropped, and we will refer to them as N and S, respectively. Combining (6) and (7), we obtain the following model:

$$THD_U(N,S) \approx \left(\sum_{i=0}^{P} k_i S^i\right) N + \sum_{j=0}^{Q} c_j S^j. \tag{8}$$

Let us, for the moment, assume that polynomial orders P and Q are known in advance. Coefficients k_i (i=0,1,…,P) and c_j (j=0,1,…,Q) can be then estimated by solving the following set of linear equations:

$$\mathbf{A}\mathbf{x} = \mathbf{b} \tag{9}$$

where

$$\mathbf{A} = \begin{bmatrix} S_{(1)}^P N_{(1)} & \cdots & S_{(1)} N_{(1)} & N_{(1)} & S_{(1)}^Q & \cdots & S_{(1)} & 1 \\ S_{(2)}^P N_{(2)} & \cdots & S_{(2)} N_{(2)} & N_{(2)} & S_{(2)}^Q & \cdots & S_{(2)} & 1 \\ \vdots & & \vdots & \vdots & \vdots & & \vdots & \vdots \\ S_{(L-1)}^P N_{(L-1)} & \cdots & S_{(L-1)} N_{(L-1)} & N_{(L-1)} & S_{(L-1)}^Q & \cdots & S_{(L-1)} & 1 \\ S_{(L)}^P N_{(L)} & \cdots & S_{(L)} N_{(L)} & N_{(L)} & S_{(L)}^Q & \cdots & S_{(L)} & 1 \end{bmatrix}$$

$$\mathbf{x} = \begin{bmatrix} k_P & \dots & k_1 & k_0 & c_Q & \dots & c_1 & c_0 \end{bmatrix}^T \tag{10}$$

$$\mathbf{b} = \begin{bmatrix} THD_U^{(1)} & THD_U^{(2)} & \dots & THD_U^{(L-1)} & THD_U^{(L)} \end{bmatrix}^T.$$

In (10), matrix **A** is of size $L\times(P+Q+2)$, whereas **x** and **b** are $(P+Q+2)\times 1$ and $L\times 1$ vectors, respectively. In addition, L represents the number of considered THD_U points. One row of matrix **A** corresponds to one THD_U point; the point indices are given in parentheses in element subscripts in matrix **A**, and element superscripts in vector **b**.

Since the number of unknown coefficients, $P+Q+2$, generally does not coincide with L, system (9) is either underdetermined or overdetermined. Recall that underdetermined linear system has either no solution or infinitely many solutions, which is not favorable in our case. Although we can consider exactly $L=P+Q+2$ points, when system (9) can be solved directly as

$$\mathbf{x} = \mathbf{A}^{-1}\,\mathbf{b}, \tag{11}$$

it is recommendable to use as many THD_U points as possible, in order to get more comprehensive solution. Therefore, we will consider $L>P+Q+2$ points, which yields overdetermined system (9). More precisely, in this paper, L will equal the total number of THD_U points obtained in simulations. Then, the vector of unknown coefficients x can be solved in the least squares (LS) sense as follows:

$$\mathbf{x} = (\mathbf{A}^T\mathbf{A})^{-1}\mathbf{A}^T\mathbf{b}. \tag{12}$$

The polynomial coefficient estimation procedure (10) and (12) should be carried out for each THD_U region separately. Alternatively, we can carry out the procedure for side (left and right) regions, while, in the middle region, the THD_U approximation can be obtained by connecting corresponding approximations from side regions.

2) *Estimation of Polynomial Orders P and Q*

The choice of polynomial orders P and Q is compromise between two contradictory requirements, namely the model accuracy and model simplicity. To that end, we will start with low orders P=1 and Q=1, and repeat the polynomial coefficient estimation procedure (10) and (12) until satisfactory THD_U accuracy is achieved. The THD_U accuracy will be evaluated through the maximal absolute relative error (MARE) calculated as

$$\text{MARE [\%]} = \max\left|\frac{THD_U(N,S) - THD_U^{est}(N,S)}{THD_U(N,S)}\times 100\right|, \tag{13}$$

where $N \in \{10, 20, \dots, 200\}$, $S \in \{3000, 4000, 5000, 6000, 7000\}$ kVA, and $THD_U^{est}(N,S)$ represents the THD_U value estimated by model. In this paper, satisfactory THD_U accuracy will be that characterized by the MARE less than 5%. The estimation of polynomial orders should be carried out for each THD_U region separately.

3) *Estimation of Middle Region Boundaries*

As already stated, at certain number of PCs, the THD_U function changes its behavior, which is reflected in larger slope value. This PC number will be referred to as the left boundary $LB(S)$. The right boundary, $RB(S)$, represents the PC number where the THD_U function again changes its behavior, taking smaller slope. Functions $LB(S)$ and $RB(S)$ will be approximated by polynomials

$$LB(S) \approx \sum_{i=0}^{B_L} l_i S^i, \qquad RB(S) \approx \sum_{j=0}^{B_R} r_j S^j, \tag{14}$$

where B_L and B_R represent the polynomial orders, and l_i and r_j represent polynomial coefficients to be estimated. Let us assume that polynomial order B_L is known in advance. Coefficients li can be then obtained by solving the following set of linear equations:

$$\mathbf{B}\,\mathbf{y} = \mathbf{c}, \tag{15}$$

where

$$\mathbf{B} = \begin{bmatrix} S_{(1)}^{B_L} & S_{(1)}^{B_L-1} & \cdots & S_{(1)} & 1 \\ \vdots & \vdots & \cdots & \vdots & \vdots \\ S_{(5)}^{B_L} & S_{(5)}^{B_L-1} & \cdots & S_{(5)} & 1 \end{bmatrix}_{5\times(B_L+1)}$$

$$\mathbf{y} = \begin{bmatrix} l_{B_L} & l_{B_L-1} & \cdots & l_1 & l_0 \end{bmatrix}^T \tag{16}$$

$$\mathbf{c} = \begin{bmatrix} N_{(1)}^{LB} & N_{(2)}^{LB} & N_{(3)}^{LB} & N_{(4)}^{LB} & N_{(5)}^{LB} \end{bmatrix}^T.$$

Matrix **B** in (16) contains five rows since we consider five S_{SC} values. Each row corresponds to one THD_U point at the left bound of middle region. In vector **c**, $N_{(k)}^{LB}$ represents the value of N that corresponds to the left boundary of the middle region for the k-th S_{SC} value. The $N_{(k)}^{LB}$ value can be readily obtained from the simulation results.

For the estimation of the right boundary $RB(S)$, the same procedure applies.

The estimation of the polynomial orders B_L and B_R will be carried out analogously to the estimation of P and Q in the previous subsection. We start with low orders B_L=1 and B_R=1, and repeat the procedure (15) and (16) until satisfactory $LB(S)$ and $RB(S)$ accuracy is achieved. In this paper, satisfactory accuracy of the $LB(S)$ and $RB(S)$ estimation is the one characterized by maximal deviation of one PC.

4) *Final results*

After estimating functions $f(S)$ and $g(S)$ according to (7)-(12), and middle region boundaries $LB(S)$ and $RB(S)$ according to (14)-(16), we obtain the THD_U model (17) given at the top of the following page.

Note that $f(S)$ is a cubic function of N in the right region, and linear function elsewhere, while $g(S)$ is linear everywhere. On the other hand, boundaries $LB(S)$ and $RB(S)$ are linear and quadratic functions of S, respectively.

Dashdot lines in Fig. 3 depict model results, showing exceptional matching between the simulations and the model. The accuracy of the proposed model is evaluated using the root mean square error (RMSE) and the MARE, calculated by (13) for fixed value of S. The results are given in Table I.

$$THD_U(N,S)=\begin{cases}(-3.043\times10^{-6}S+5.44\times10^{-2})N-4.527\times10^{-4}S+4.714, & \text{for } N\le LB(S),\\ (-2.931\times10^{-7}S+1.059\times10^{-1})N-1.348\times10^{-3}S+3.916, & \text{for } LB(S)<N<RB(S),\\ (-7.647\times10^{-13}S^3+1.219\times10^{-8}S^2-6.701\times10^{-5}S+1.767\times10^{-1})N-5.264\times10^{-4}S+4.466, & \text{for } N\ge RB(S)\end{cases}$$

$$LB(S)=1\times10^{-2}S+30 \qquad (17)$$

$$RB(S)=-5\times10^{-7}S^2+1.35\times10^{-2}S+34.$$

TABLE I. ESTIMATION ERROR OF THE PROPOSED MODEL QUANTIFIED BY THE RMSE AND MARE

S_{SC}	RMSE	MARE
3000	0.0899	2.55
4000	0.0900	3.04
5000	0.0705	4.40
6000	0.0799	2.77
7000	0.0567	4.21

Finally, the error in the estimation of middle region boundaries $LB(S)$ and $RB(S)$ is by far below the preset limit of one PC. The maximal error in the estimation of both $LB(S)$ and $RB(S)$ is of order 10^{-10}.

V. Validity of the Proposed Model

In order to evaluate the validity of the proposed model, a measurement session was performed in a commercial bank building (NLB Montenegrobanka, Podgorica, Montenegro), in September 2012. The building is equipped with 243 modern PCs (221 personal PCs and 22 server PCs of total active power of 37.6 kW).

Two measurement sites were in the focus: the first one, feeder in TS 10/04, which supplies the bank building, and the second one, the PCC in the bank building, from which a group of PCs is supplied. Beside the PCs, additional, smaller linear non-PC loads, such as fluorescent lamps and water heaters, were switched on during the measurements.

The first measurement set was necessary in order to record the pre-existing THD_U value and to determine the S_{SC} value. The recorded values of the pre-existing THD_U (per phases) were 1.90%, 1.75% and 1.82%. The calculated value of the grid stiffness was S_{SC} = 5800 kVA (about 45% greater value than that of the CCFTS). The PCC in the bank building supplies 83, 80 and 81 PCs, connected per phases 1, 2, 3, respectively. The recorded RMS values of the phase and neutral currents were 44.6 A, 42.9 A, 43.1 A and 38.6 A. Compared with the results from the CCFTS, it can be concluded that the PC consumption in the bank is lower than that in the CCFTS. Also, the neutral current value (38.6 A) is lower than in the CCFTS, although, again, it is close to the value of phase currents.

What matters the most, the measured THD_U value of the most loaded phase is THD_U = 4.92%. If model (16) is used with N_{PC} = 83 and S_{SC} = 5800 kVA, the value of THD_U = 5.14% is obtained, which confirms the validity of the model. Note here that the small discrepancy between the measurement and model results is due to linear non-PC loads, which decrease the measured THD_U value.

VI. Discussion

The proposed model (17) can be further analyzed by taking into account the following effects:

A. Effects of the Cable Cross-Section

Cable PP-Y 5×4 mm^2, length of about 80 m, supplies the PCC of the CCFTS. Simulation model, and in turn analytical model (17), are obtained for such a cable. The maximal current capacity of the mentioned cable is I_{max} = 47 A. For a larger PC cluster, i.e., larger values of generated current, greater cable cross-section is needed. Hence, it is very important to analyze the THD_U dependence on the cable cross-section to see whether the introduction of cable cross-section as an additional parameter in model (17) is necessary.

For a given cable length and grid stiffness of S_{SC} = 4000 kVA, the THD_U increases with the increase of the cable cross-section. This is due to the fact that at larger cross-section the distances between the neutral conductor and the phase conductors is increased leading to respective increase of the neutral conductor impedance. However, for different cable cross-sections, namely 5×6 mm^2, 5×10 mm^2, 5×16 mm^2 and 5×25 mm^2, which are very common in practice, the deviations of the THD_U values from model (17), expressed in terms of the RMS in Table II, do not exceed 1.83%.

For the case of cross-section of 5×25 mm^2 and grid stiffnesses of 6000 kVA and 7000 kVA, the considered effect is much less pronounced, i.e., maximal deviations are 1.34% and 1.07%, respectively. Slightly larger deviations (3.63%) are obtained for very low grid stiffness of S_{SC} = 3000 kVA. The influence of the cable cross-section on the THD_U, therefore, can be practically neglected.

TABLE II. RMS OF DEVIATION OF SIMULATED THD_U VALUES (OBTAINED FOR VARIOUS CABLE CROSS-SECTIONS) FROM THE MODEL THD_U VALUES. FIXED S_{SC} = 4000 KVA IS CONSIDERED

Cross-section (mm^2)	N_{PC}				
	10	50	100	150	200
5×6	0.10%	0.21%	0.39%	0.55%	0.71%
5×10	0.16%	0.29%	0.51%	0.72%	1.03%
5×16	0.23%	0.38%	0.72%	1.08%	1.42%
5×25	0.35%	0.73%	1.15%	1.40%	1.83%

B. Effects of the pre-existing THD_U

The initial model conditions must match real grid conditions as much as possible. The PC cluster at the CCFTS is connected on the low voltage PCC, where the initial THD_U of phase voltages exist. The measured pre-existing THD_U values are incorporated within the simulation model, that was a base for developing final mathematical model (17). However, in order to preserve the model simplicity, the pre-existing THD_U is not taken as a parameter. Now, a question of validity of such a decision arises. It is shown in section V that model (17) for the case of pre-existing THD_U of 1.9% (as opposed to 2.1% adopted in the model), gives results very close to the measured ones, with difference less than 0.2%. Also, simulations carried out with the pre-existing THD_U values of 1.75%, 1.82%, 2.18%

and 2.25% and constant S_{SC} and N_{PC} values, show a slight difference between the obtained results (the maximal discrepancy was 0.89%). This points to the fact that common values of the pre-existing THD_U on the low voltage level (1.5-2.5%) have insignificant impact on the model accuracy.

C. Influence of load-side parameters

The simulation model used in this paper takes into account the technology structure of modern PCs. From the power quality point of view, the power supply unit (PSU) is the most significant PC component. More precisely, capacitors within the PSU (usually two capacitors connected in parallel [1], [10]) represent the major harmonic source, which can affect the total current harmonic distortion (THD_I), as shown in [10], and its influence decreases with the increase of the PC cluster size.

Simulations carried out in this paper, that take into account a wide range of the PSU capacitances encountered in modern PCs (235-500 µF), show that the influence of the PSU capacitance on the THD_U can be neglected. Therefore, we have omitted it in the final THD_U model (17).

VII. Conclusions

The exact determination of voltage distortion, quantified with the THD_U, is of great importance. Comparing THD_U value with the THD_U limits defined by relevant standards, information about consumers potential effect on voltage quality may be obtained. This paper considers mathematical modeling of the THD_U caused by simultaneous operation of PC cluster. In addition to the THD_U dependence on the PC cluster size, the proposed model takes into account a strong dependence of the THD_U on the grid stiffness. The effects of the cable cross-section and pre-existing THD_U of phase voltage on the model are discussed, concluding that they are not significant and can be neglected. The same applies to the influence of line-side parameters (PSU capacitance in the first place). Measurement and simulation results were the bases for developing the THD_U model, whose coefficients are derived in the least squares sense. The accuracy of the model is verified using additional measurements.

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